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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,844	JEDDELOH, JOSEPH M.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☒ Claim(s) *1-22 and 32-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03-3/28/06*. 04/20/04, 02/26/04, 05/17/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed April 05, 2004 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Information Disclosure Statement

Applicant's Information Disclosure Statements, filed on 6/17/2005, 2/06/2006, and 4/25/2006 have been received, and entered into the record.

However, It is impractical for the examiner to review the references thoroughly with the number of references cited in this case. By initializing each of the cited references on the accompanying 1449 forms, the examiner is merely acknowledging the submission of the cited references and merely indicating that only a cursory review has been made of the cited references.

MPEP § 2004.13 states:

> "It is desirable to avoid the submission of long lists of documents if it can be avoided. Eliminate clearly irrelevant and marginally pertinent cumulative information. If a long list is submitted, highlight those documents which have been specifically brought to applicant's attention and/or are known to be of most significance.

See Penn Yan Boats, Inc. v. Sea Lark Boats, Inc., 359 F. Supp. 948, 175 USPQ 260 (S.D. Fla. 1972), aff 'd, 479 F.2d 1338, 178 USPQ 577 (5th Cir. 1973), cert. denied, 414 U.S. 874 (1974). But cf. Molins PLC v. Textron Inc., 48 F.3d 1172, 33 USPQ2d 1823 (Fed. Cir. 1995)."

Further, it should be noted that an applicant's duty of disclosure of material and information is not satisfied by presenting a patent examiner with "a mountain of largely irrelevant [material] from which he is presumed to have been able, with his experience and with adequate time, to have found the critical [material]. It ignores the real world conditions under which examiners work." Rohm & Haas Co. v. Crystal Chemical co., 722 F.2d 1556, 1573 [220 USPQ 289] (Fed. Cir. 1983), cert. Denied, 469 U.S. 851 (1984). Patent applicant has a duty not just to disclose pertinent prior art references but to make a disclosure in such a way as not to "bury" it within other disclosures of less relevant prior art; see Golden Valley Microwave Foods Inc. v. Weaver Popcorn Co. Inc., 24 USPQ2d 1801 (N.D. Ind. 1992); Molins PLC v. Textron Inc., 26 USPQ2d 1889, at 1899 (D.Del 1992); Penn Yan Boats, Inc. v. Sea Lark Boats, Inc. et al., 175 USPQ 260, at 272 (S.D. Fl. 1972).

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1-50 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-50 of copending Application No. 11/431437. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Objections

Claims 19-22 & 32-35 are objected to because of the following informalities:

As per claim 19 & 32:

These claims are objected to as the claim mentions "operable couple," whereas it should mention operable to couple.

As per claims 20-22 & 33-34:

These claims are rejected by virtue of its dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18, 23-31, 36-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 11, 23, 36, 42, & 44:

These claims mention the term "relative timing." The term relative is indefinite and it does not clearly point out the subject matter of the invention.

As per claims 2-10, 12-18, 24-31, 37-41, & 43:

These claims are rejected by virtue of its dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-6, 10-11, 13-15, 19 & 22 are rejected under 35 U.S.C. 102 (e) as being fully anticipated by Lin et al. (hereinafter Lin) US Pat no. 6880117 B2.

As per claims 1 & 11:

Lin teaches a memory module, comprising: a plurality of memory devices (Figure 2 # 50A-c); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to

the memory device and coupling read data from the memory device (Figure 4A); and a self-test module (Figure 1 # 22) coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range (Figure 1 # 24), the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals (Figure 1 # 34).

As per claim 3 &13:

Lin teaches the memory module as rejected in claim 1 above wherein the memory hub further comprises a plurality of link interfaces (Figure 2 # 40, 42, 44), a plurality of memory device interfaces (Figure 2 # 50A-C), and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces (column 8, lines 5-60).

As per claim 4 & 14:

Lin teaches the memory module as rejected in claim 1 above wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices (column 2, lines 55-60).

As per claim 5:

Lin teaches the memory module as rejected in claim 1 above wherein the self-test module further comprises: a pattern generator producing a pattern of

data bits each of which is used to generate a respective one the first signals in the series (Figure 1 # 32); and a comparator coupled to the pattern generator and to the at least one memory device, the comparator receiving output signals from the at least one memory device and determining a pattern of data corresponding thereto, the comparator further and comparing the pattern generated from the output signals to the pattern of data from which the first signals are generated (Figure 1 # 34).

As per claim 6 & 15:

Lin teaches the memory module as rejected in claim 1 above wherein the self-test module further comprises a storage device coupled to the comparator to store the results of the comparisons between the pattern generated from the output signals and the pattern of data from which the first signals are generated (Figure 1 # 30, column 5, lines 5-40).

As per claim 10:

Lin teaches the memory module as rejected in claim 1 above wherein the self-test module is further operable to couple a signal from the memory device corresponding to each of the output signals and to alter the relative timing between the signal coupled from the memory device and the corresponding output signal (Figure 1 # 24 & 28).

As per claim 19:

Lin teaches a memory module, comprising: a plurality of synchronous memory devices (Figure 2 # 50A-C); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory

devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 24); and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 24, column 4, lines 15-65)), the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 34).

As per claim 22:

Lin teaches the memory module as rejected in claim 19 above wherein the memory hub further comprises a plurality of link interfaces (Figure 2 # 40, 42, 44), a plurality of memory device interfaces (Figure 2 # 50A-C), and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces (column 8, lines 5-60).

Claims 1, 11, & 19 are rejected under 35 U.S.C. 102 (b) as being fully anticipated by Pierce et al. (Pierce) US PG Pub no. 20010013110 A1.

As per claims 1, 11 & 19:

Pierce teaches a memory module, comprising: a plurality of synchronous memory devices (Figure 1 # 12); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 22); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 40); and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 40), the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 10).

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2, 9, 12, 16-17, 20-21, 23 & 32 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Lin et al. US Pat no. 6880117 B2.

As per claim 2 & 12, 21:

Lin discloses the claimed invention except for the exact location of the maintenance port. It would have been obvious to one having ordinary skill in the art at the time the invention was made to place the maintenance port such that it was externally accessible, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 9, 16-17, 20:

Lin discloses the claimed invention except for explicitly mentioning the exact composition of the first and second signals. It would have been obvious to one of ordinary skill in the art at the time the invention was made to comprise the first signals with data (Figure 1 "Test Data"), and the second signal to comprise of data strobe (Figure 1 "Strobe"), since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 23:

Lin substantially teaches a memory module, comprising: a plurality of memory devices (Figure 2 # 50A-c); and a memory hub, comprising: a link

interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 4A); and a self-test module (Figure 1 # 22) coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range (Figure 1 # 24), the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals (Figure 1 # 34), at least one input device coupled to the peripheral device port of the system controller (Figure 1 # 32); at least one output device coupled to the peripheral device port of the system controller (Figure 1 # 38) and at least one data storage device coupled to the peripheral device port of the system controller (Figure 1 # 30).

Lin does not explicitly mention that processor having a processor bus or a system controlled having a system memory port and a peripheral device port. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to realize that the apparatus taught in Lin generally includes standard equipment like a processor, processor bus, a controller, and

various input/output ports. Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to use the mentioned apparatus since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Further it should be noted that the tester (Figure 1 # 22) could be used within Lin's invention to perform the exact same functions as the apparatus mentioned in claim 23. Hence these should be considered as art recognized equivalents.

As per claims 32:

Lin substantially teaches a memory module, comprising: a plurality of synchronous memory devices (Figure 2 # 50A-C); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 24); and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 24, column 4, lines 15-65)), the self-test module further being operable couple a series of first

input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 34), at least one input device coupled to the peripheral device port of the system controller (Figure 1 # 32); at least one output device coupled to the peripheral device port of the system controller (Figure 1 # 38) and at least one data storage device coupled to the peripheral device port of the system controller (Figure 1 # 30).

Lin does not explicitly mention that processor having a processor bus or a system controlled having a system memory port and a peripheral device port. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to realize that the apparatus taught in Lin generally includes standard equipment like a processor, processor bus, a controller, and various input/output ports. Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to use the mentioned apparatus since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Further it should be noted that the tester (Figure 1 # 22) could be used within Lin's invention to perform the exact same functions as the apparatus mentioned in claim 23. Hence these should be considered as art recognized equivalents.

Claims 7-8, 24-31, 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable under Lin et al. US Pat no. 6880117 B2 and further in view of Sine et al. US Pat no. 5621739.

As per claims 7 & 8:

Lin substantially teaches a memory module, comprising: a plurality of memory devices (Figure 2 # 50A-c); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 4A); and a self-test module (Figure 1 # 22) coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range (Figure 1 # 24), the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals (Figure 1 # 34), wherein the self-test module comprises a memory sequencer coupled to the at least one memory device, the memory sequencer generating and coupling to at least one memory device a

sequence of control signals to cause the at least one memory device to respond to each of the first and second signals in the series (Figure 2 # 48).

Lin does not explicitly teach the delay line coupled to the BIST.

However, Sine et al. in an analogous art teaches a delay line coupled to a BIST (Figure 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a delay line within the tester of Lin, since that would enable Lin's apparatus to make use of the benefits of delay testing. Further it should be noted that the timing generator/frequency multiplier (Figure 1) could be used within Lin's invention as a delay line. Hence these should be considered as art recognized equivalents.

As per claims 24-31:

These claims teach the same limitations as claims 2-10. Therefore these claims are rejected under the same basis as mentioned above.

As per claims 33-35:

These claims teach the same limitations as claims 20-22. Therefore these claims are rejected under the same basis as mentioned above.

As per claims 36-50:

Claims 36-50 are directed to a method of the system and memory modules of claims 1-35. Lin and Sine teach, either alone or in combination as stated above, the system and memory modules as set forth in claims 1-35. Therefore, Lin and Sine also teach, either alone or in combination as stated above, the methods as set forth in claims 36-50.

Claims 23, 32, 36, 42, 44, & 45 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Pierce US PG-Pub no. 2001/0013110 A1.

As per claims 23 & 32:

Pierce substantially teaches a memory module, comprising: a plurality of synchronous memory devices (Figure 1 # 12); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 22); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 40); and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 40), the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 10), at least one input device coupled to the peripheral device port of the system controller (Figure 1 # 14); at least one output device coupled to the peripheral device port of the system

controller (Figure 1 # 20) and at least one data storage device coupled to the peripheral device port of the system controller (Figure 4 # 308).

Pierce does not explicitly mention that processor having a processor bus or a system controlled having a system memory port and a peripheral device port. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to realize that the apparatus taught in Pierce generally includes standard equipment like a processor, processor bus, a controller, and various input/output ports. Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to use the mentioned apparatus since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Further it should be noted that the tester (Figure 1 # 22) could be used within Pierce's invention to perform the exact same functions as the apparatus mentioned in claim 23. Hence these should be considered as art recognized equivalents.

As per claims 36, 42, 44, & 45:

Claims 36, 42, 44 & 45 are directed to a method of the system and memory modules of claims 1, 11, 19, 23 & 32. Pierce teaches as stated above, the system and memory modules as set forth in claims 1, 11, 19, 23 & 32. Therefore, Pierce also teaches as stated above the methods as set forth in claims 36, 42, 44, & 45.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US PG-Pub no. (20020199139 A1, 20020046379 A1, 20030226072 A) and US Pat no. 7036055 B2 mention the same self-test module sending multiple signals are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
06/22/2006

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100